What is claimed is:

[Claim 1] 1. An integrated circuit comprising:

a substrate of a first polarity;
a trench structure in said substrate;
a well region of a second polarity abutting said trench structure; and
a heavily doped region of said second polarity abutting said trench structure, wherein said heavily doped region having a dopant concentration greater than a dopant concentration of said well region, and wherein said heavily doped region is adapted to suppress latch-up in said integrated circuit.

[Claim 2] 2. The integrated circuit of claim 1, wherein said heavily doped region comprises a sub-collector region.

[Claim 3] 3. The integrated circuit of claim 1, further comprising a shallow trench isolation region, wherein said trench structure comprises a deep trench structure having a depth and a width, wherein said depth is at least twice as large as said width, and wherein said shallow trench isolation region is over said deep trench structure.

[Claim 4] 4. The integrated circuit of claim 3, wherein an aspect ratio of said depth to said width is at least 2.85.

[Claim 5] 5. The integrated circuit of claim 1, further comprising a shallow trench isolation region, wherein said trench structure comprises a trench isolation region having a depth and a width, wherein said depth is at least twice as large as said width, and wherein said trench isolation region traverses said shallow trench isolation region.

[Claim 6] 6. The integrated circuit of claim 5, wherein an aspect ratio of said depth to said width is at least 2.5.

[Claim 7] 7. The integrated circuit of claim 1, further comprising:

a p+ anode in said well region;
a n+ cathode in said well region; and
a gate structure over said p+ anode and said n+ cathode.

[Claim 8] 8. A complementary metal oxide semiconductor (CMOS) device, said CMOS device comprising:

a p-type substrate;
shallow trench isolation regions in said p-type substrate;
p-type diffusion regions in said p-type substrate and in between successive ones of said STI regions;
a n-type retrograde well in said p-type substrate;
a deep trench isolation region bounding said p-type diffusion regions and said n-type retrograde well; and
a n-type sub-collector adjacent to a sidewall of said deep trench isolation region and below said STI regions,
wherein said p-type diffusion regions, said n-type retrograde well, and said p-type substrate form a pnp parasitic bipolar transistor in said CMOS device, and wherein said deep trench isolation region and said n-type sub-collector are adapted to suppress latch-up in said CMOS device that is caused by said pnp parasitic bipolar transistor.

[Claim 9] 9. The CMOS device of claim 8, wherein said n-type sub-collector comprises a uniform dopant layer.

[Claim 10] 10. The CMOS device of claim 8, wherein said n-type sub-collector comprises a discontinuous dopant layer.

[Claim 11] 11. The CMOS device of claim 8, wherein said n-type sub-collector is adjacent to a lower surface of said n-type retrograde well.

[Claim 12] 12. The CMOS device of claim 8, wherein said deep trench isolation region comprises a depth and a width, wherein said depth is at least twice as large as said width, and wherein said shallow trench isolation regions are over said deep trench isolation region.

[Claim 13] 13. A method of forming an integrated circuit, said method comprising:

forming a substrate of a first polarity;
forming a trench structure in said substrate;
forming a well region of a second polarity abutting said trench structure; and configuring a heavily doped region of said second polarity abutting said trench structure, wherein said heavily doped region having a dopant concentration greater than a dopant concentration of said well region, and wherein said heavily doped region suppresses latch-up in said integrated circuit.

[Claim 14] 14. The method of claim 13, wherein in said configuring of said heavily doped region of said second polarity, said heavily doped region comprises a sub-collector region.

[Claim 15] 15. The method of claim 13, further comprising configuring a shallow trench isolation region in said substrate, wherein said trench structure is configured as a deep trench structure having a depth and a width, wherein said depth is at least twice as large as said width, and wherein said shallow trench isolation region is configured over said deep trench structure.

[Claim 16] 16. The method of claim 15, wherein an aspect ratio of said depth to said width is at least 2.85.

[Claim 17] 17 The method of claim 13, further comprising:

forming a p+ anode in said well region;
forming a n+ cathode in said well region; and
forming a gate structure over said p+ anode and said n+ cathode.

[Claim 18] 18. A method of forming an integrated circuit, said method comprising:

forming a substrate of a first polarity;
forming a well region of a second polarity in said substrate;
configuring a heavily doped region of said second polarity in said substrate, wherein said heavily doped region comprises a dopant concentration greater than a dopant concentration of said well region; and
forming a trench structure in said substrate and through said well region and said heavily doped region, wherein said trench structure and heavily doped region suppresses latch-up in said integrated circuit.

[Claim 19] 19. The method of claim 18, wherein in said configuring of said heavily doped region of said second polarity, said heavily doped region comprises a sub-collector region.

[Claim 20] 20. The method of claim 18, further comprising configuring a shallow trench isolation region in said substrate, wherein said trench structure is configured as a trench isolation region having a depth and a width, wherein said depth is at least twice as large as said width, and wherein said trench isolation region traverses said shallow trench isolation region.

[Claim 21] 21. The method of claim 20, wherein an aspect ratio of said depth to said width is at least 2.5.

[Claim 22] 22. The method of claim 18, further comprising:

forming a p+ anode in said well region;
forming a n+ cathode in said well region; and
forming a gate structure over said p+ anode and said n+ cathode.